

FORM 1449*

INFORMATION DISCLOSURE STATEMENT

IN AN APPLICATION

(Use several sheets if necessary)

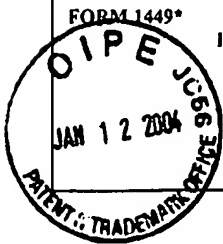
Docket Number:

10873.1318US01

Application Number:

10/686,826

Applicant: KURUMADA, et al.

Filing Date: October 15,
2003Group Art Unit: ~~Unknown~~
2813

U.S. PATENT DOCUMENTS

| EXAMINER INITIAL | DOCUMENT NO. | DATE | NAME | CLASS | SUBCLASS | FILING DATE IF APPROPRIATE |
|---------------------|--------------|--------------|--------------|-------|----------|-------------------------------|
| CAI | 6,212,117 | April, 2001 | Shin, et al. | — | — | |
| CAI | 6,434,074 | August, 2002 | Brown | — | — | |
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FOREIGN PATENT DOCUMENTS

| | DOCUMENT NO. | DATE | COUNTRY | CLASS | SUBCLASS | TRANSLATION | |
|---|--------------|------|---------|-------|----------|-------------|----|
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | |
|-----|---|
| CAI | Osada, et al., "Universal- V_{dd} 0.65-2.0-V 32-kB Cache Using a Voltage-Adapted Timing-Generation Scheme and a Lithographically Symmetrical Cell", Journal of Solid-State Circuits, vol. 36, no. 11, November, 2001, pages 1738-1744 |
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23552

PATENT TRADEMARK OFFICE

EXAMINER

Craig A. Johnson

DATE CONSIDERED

3/20/05

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form for next communication to the Applicant.